

(19) World Intellectual Property
Organization
International Bureau



(43) International Publication Date
26 May 2005 (26.05.2005)

PCT

(10) International Publication Number
WO 2005/048318 A3

(51) International Patent Classification⁷: **H01L 29/94**

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(21) International Application Number:
PCT/US2004/038582

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(22) International Filing Date:
17 November 2004 (17.11.2004)

(81) Designated States (unless otherwise indicated, for every kind of national protection available): AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, MZ, NA, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RU, SC, SD, SE, SG, SK, SL, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, YU, ZA, ZM, ZW.

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
60/520,322 17 November 2003 (17.11.2003) US
60/527,306 8 December 2003 (08.12.2003) US

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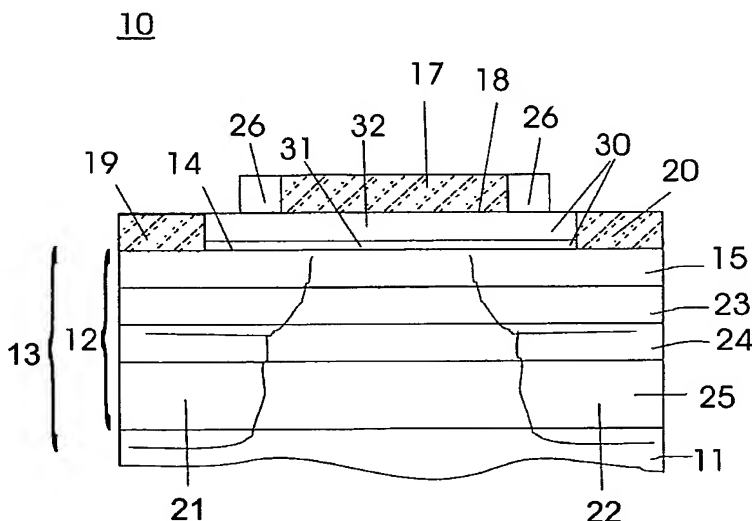
(84) Designated States (unless otherwise indicated, for every kind of regional protection available): ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LU, MC, NL, PL, PT, RO, SE,

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[Continued on next page]

(54) Title: NITRIDE METAL OXIDE SEMICONDUCTOR INTEGRATED TRANSISTOR DEVICES



(57) Abstract: A self-aligned enhancement mode or depletion mode nitride based metal-oxide-compound semiconductor field effect transistor (10) includes a gate insulating structure comprised of a first oxide layer that in comprised of gallium oxides or indium oxides compounds (30) positioned immediately on top of the nitride compound semiconductor structure, and a second insulating layer comprised of either (a) oxygen and rare earth elements, (b) gallium oxygen and rare earth elements, or (c) gallium+indium and rare earth elements positioned immediately on top of said first layer. Together the lower indium oxide or gallium oxide layer and the second insulating layer form an epitaxial oxide gate insulating structure. The gate insulating structure and underlying compound semiconductor layer (15) meet at an atomically abrupt interface at the surface of with the compound semiconductor wafer structure (14) that is

based on the nitride family of compound semiconductors. The first oxide layer serves to passivate and protect the underlying compound semiconductor surface from the second insulating layer and atmospheric contamination. A refractory metal gate electrode layer (17) is positioned on upper surface (18) of the second insulating layer. The refractory metal is stable on the second insulating layer at elevated temperature. Self-aligned source and drain areas, and source and drain contacts (19, 20) are positioned on the source and drain areas (21, 22) of the device. Multiple devices are then positioned in proximity and the appropriate interconnection metal layers and insulators are utilized in concert with other passive circuit elements to form an integrated circuit structure. Finally, NMOS and PMOS nitride based devices are positioned in proximity to for a complementary metal oxide semiconductor integrated circuit in nitride based compound semiconductors.

WO 2005/048318 A3



SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:

- *with international search report*
- *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

(88) Date of publication of the international search report:
15 December 2005

(15) Information about Correction:

Previous Correction:

see PCT Gazette No. 25/2005 of 23 June 2005, Section II

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.